Requirements and Security Challenges for Resource-Constrained IoT End-Devices Baseband Processor

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Introduction: IoT devices (1/2)

- Number of Internet of Things (IoT) devices expanding exponentially
  (+10 Billions, in 2021; [Jovanović and Vojinovic, 2021])
- A wide range of applications and use-cases
  (ex: healthcare, industry and agriculture)
- Multiple constraints on resources are related to IoT devices
  (energy, communication range, data rate, flexibility, life-cycle,. . .)

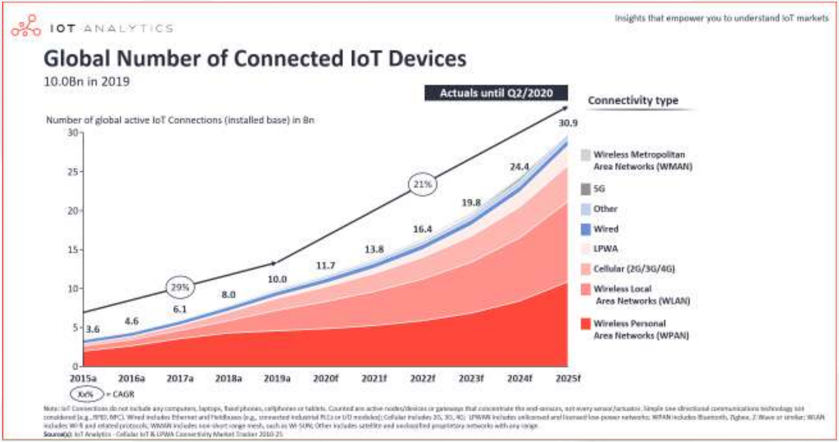

Figure: Global number of connected IoT devices [IoT, 2020]

Introduction: Wireless Connectivity in IoT (1/2)

- Explosion of number of IoT device connections (+20 Billions in 2019) [IoT, 2020])
- Emergence of a large number of IoT standards and protocols
- Development of Low Data Rate and Low Power protocols to match the challenges of the IoT environment (LoRa, BLuetooth/BLE, NB-IoT, Zigbee, SigFox, . . .)

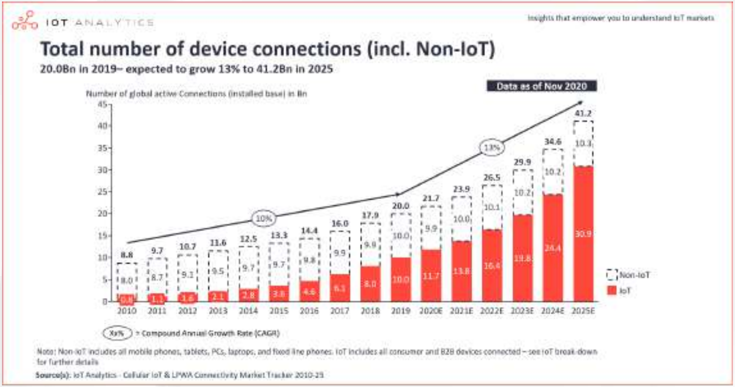

Figure: Total number of device connections (incl. Non-IoT) [IoT, 2020]

Motivation and Identified challenges

- Several challenges resulting from the evolution of IoT infrastructures (number of devices, waveforms and communication protocols).

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- New approaches to implement the physical layer using Software Defined Radio (SDR) architecture are proposed to reach flexibility and multi-protocol operations.

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- The implementation of wireless connectivity using (SDR) could expand the attack surface for traditional security exploits (ROP, Overflow, . . .).

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- The implementation of wireless connectivity using (SDR) could expand the attack surface for traditional security exploits (ROP, Overflow, . . .).
- Various requirements and challenges have to be considered in the design of IoT devices: Security, Flexibility and Power Consumption

Security of embedded systems?

- Physical Access
- Cryptography Implementation
- ...
- Network Entry Point

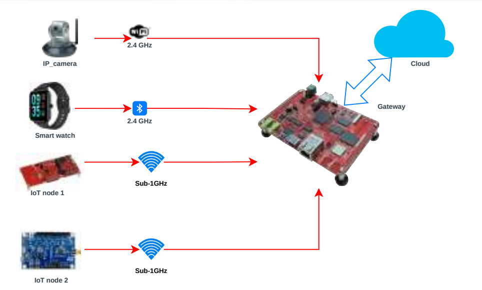

Figure: IoT architecture

Objectives

- Focus on wireless connectivity of resource-constraints IoT devices

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- Focus on RISC-V open source ISA for BaseBand/Network CPU

SoC for IoT overview

- Main CPU for application user

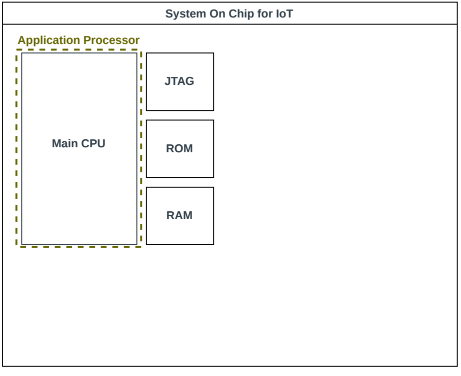
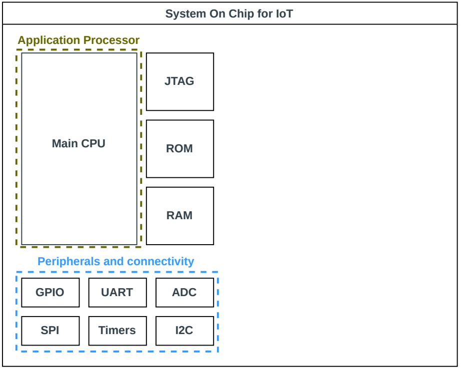


Figure: SoC IoT overview

SoC for IoT overview

- Main CPU for application user
- Peripherals and connectivity



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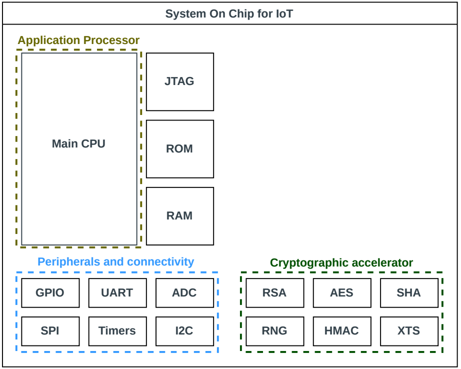

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SoC for IoT overview

- Main CPU for application user
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- Integration of protection mechanisms
- Isolation between Radio and user application

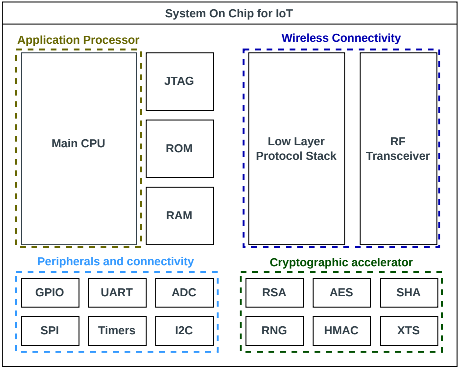

Figure: SoC IoT overview

Don't forget that SoC are integrating a wireless connectivity unit!

Baseband architecture: Dedicated Hardware

- ESP32-C3 from Espressif
- Dedicated hardware (Baseband part) for each waveform / Protocol
- Lack of flexibility

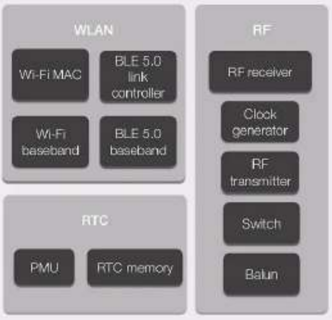

Figure: Wireless Connectivity of ESP32-C3

Baseband architecture: CPU + DSP

- Generic CPU based architecture (Without ISA extension)
- Integration of a DSP for the radio part

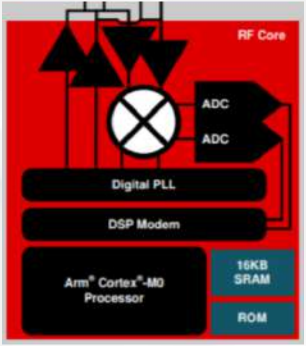

Figure: wireless connectivity of CC1352R

- Hybrid FPGA (Zynq) or FPGA + MCU

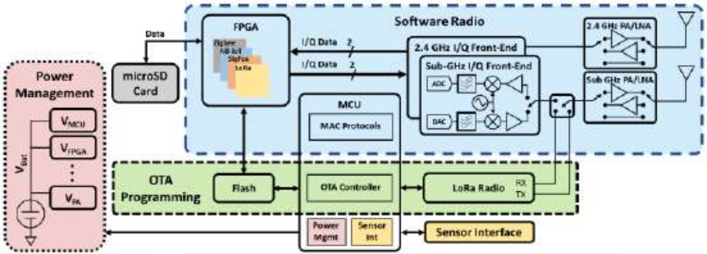

Figure: SoC TinySDR [Hessar et al., 2020]

- CPU Dedicated architecture

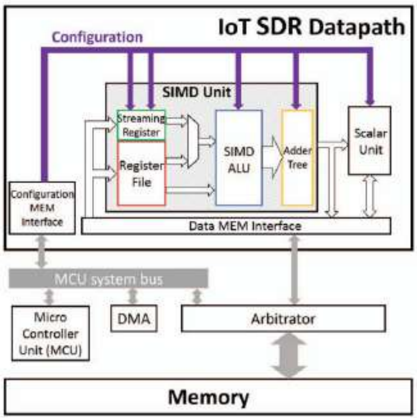

Figure: SMID based CPU Dedicated Architecture [Chen et al., 2016]

- CPU with ISA extension (ARM, RISC-V)

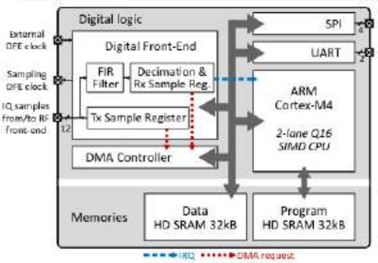

Figure: Architecture ARM
[Xhonneux et al., 2021]

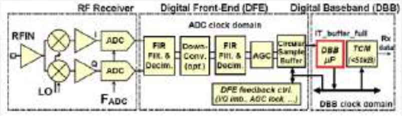

Figure: Architecture RISC-V
[Amor et al., 2019, Belhadj Amor et al., 2021]

Examples of SoC in industry

- Texas instruments
- ST Microelectronics
- NXP
- Espressif
- . . .

Figure: CC1352R SoC Texas instruments

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Figure: CC1352R SoC Texas instruments

Several SoCs in industry include a core dedicated to wireless connectivity

Challenges and identified marks

- A software-defined baseband radio processor using a generic CPU architecture with an instruction set extension is more interesting.
- The constraints of limited resources and consumption of connected objects must be taken into account.
- Other challenges associated with the software radio must also be taken into account: security, programmability

Baseband	Dedicated Hardware	Hybrid FPGA	CPU (dedicated)	CPU (Generic)
Multi-Protocol	✗	✓	✓	✓
Programmability	✗	+	+	+++
Security Mechanism	✗	✗	✗	✗
Flexibility	✗	+++	+	++
Dynamic power	$\sim$ 100mW	$\sim$ 100mW	$\sim$ 10mW	$\sim$ 10μW

Table: A comparison of IoT SDR baseband processor architectures and their features

Threat Model

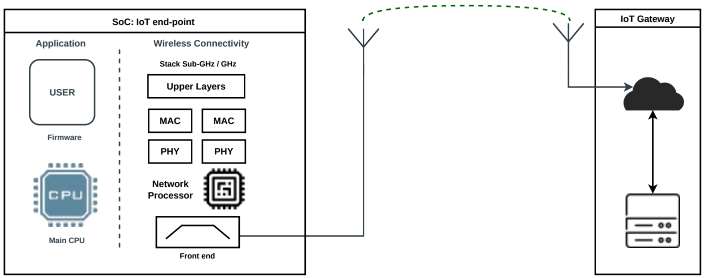
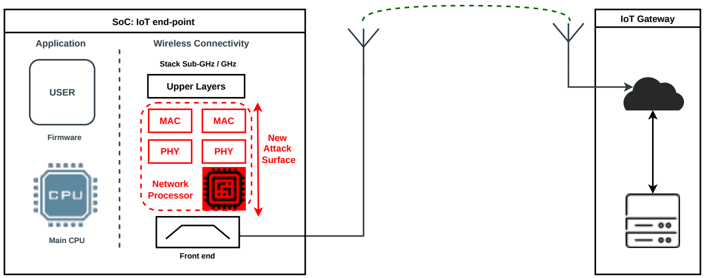


Figure: Potential Threat Model

Target : Remote Attacks

Threat Model



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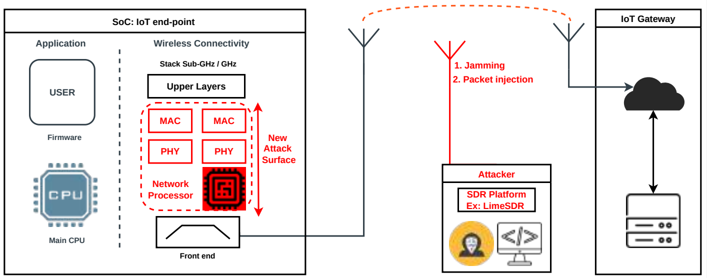


Figure: Potential Threat Model

Target : Remote Attacks

- Jamming Attack
- Logical Attacks: Packet Injection, . . .

Vulnerabilities in IoT

Vulnerability	AMNESIA33	BLEEDINGBIT	LoRaDawn
Number of CVEs	33 [Labs, 2020]	2 [Seri, Benn (ARMIS et al., 2019]	2 [ten, 2020]
Where ?	Poor Software Development	Masking Error, OAD	OTAA Process, 32bit Gateway
Target Device	uIP, FNET, picoTCP, NuTNet	AP with TI BLE	LoRaMac-node, LoRa Basics Station
Stack Layer	Physical /MAC	MAC	MAC
Stack / protocol	TCP/IP / IEEE 802.15.4	BLE	LoRaWAN
Exploit	RCE, DoS, Steal Data	Packet injection, RCE	DoS, RCE, Heap UAF

Table: A set of three Groups of vulnerabilities in IoT and their features

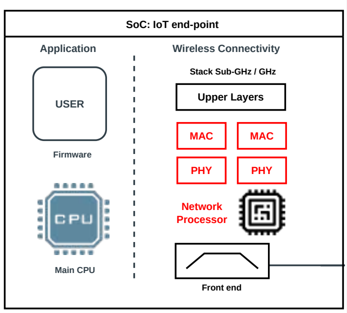


Figure: SoC for IoT with wireless connectivity

- Vulnerabilities: Long synchronization time between Slave and Master BLE in connection step
- Exploit: Packet injection (Hijacking slave and master, MITM)
- InjectBLE Firmware
- Mirage framework
- Used BLE module: nRF52840-dongle

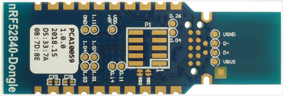


Figure: nRF52840-dongle : `https://www.nordicsemi.com/`

We reproduce the MITM attack using two modules from mirage framework in order to sniff packets between master and slave: (ble_hijack and ble_master)

- ble_master: Mobile App
- ble_slave: Led strip
- Attacker: Laptop with nRF52840-dongle

Figure: Sniffing packet exploit

Example of Exploit: Packet Injection

After hijacking the BLE Master we perform a packet injection exploit

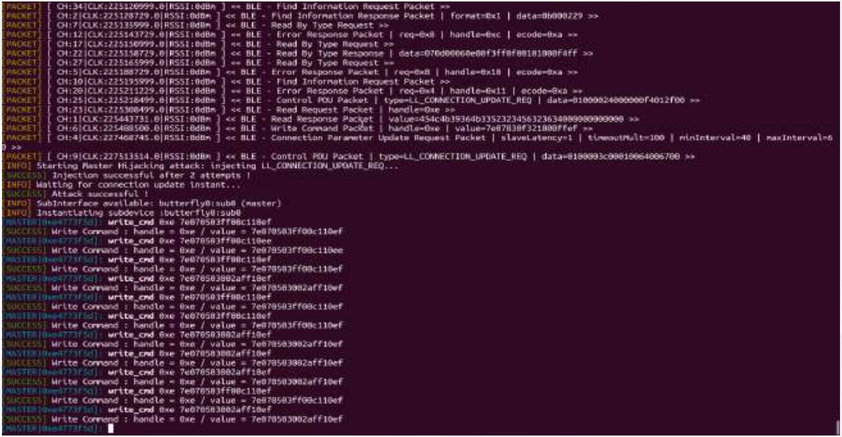
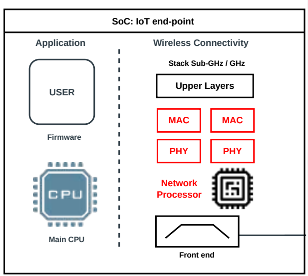


Figure: Packet Injection exploit



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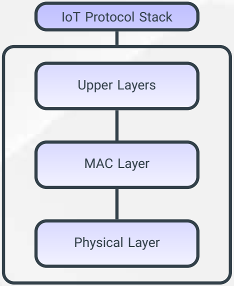
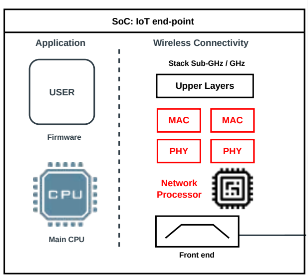


Figure: IoT protocol stack layers

Attacks in IoT



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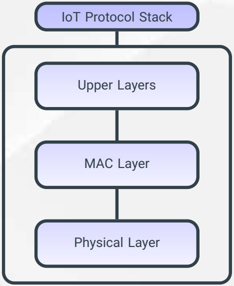

Figure: IoT protocol stack layers

E (Exploited Layer) **T** (Targeted Layer)

Ref	Protocol	Attack	PHY	MAC	Upper	Exploit
[Cayre et al.,]	Zigbee	Wazabee	E	E/T	T	DoS, packet injection
[Aras et al.,]	LoRaWAN	Selective Jamming	E	E/T	T	DoS, Wormhole
[Hessel et al.,]	LoRaWAN	Spoofing	E	E/T	-	DoS
[Avoine and Ferreira, 2018]	LoRaWAN		-	T	T	replay, decrypt, DoS
[Cayre et al., 2021]	BLE	InjectBLE	E	E/T	T	MITM, Sniffing
[Zhang et al., 2020]	BLE	Downgrade	-	-	T	DoS, MITM
[Santos et al., 2019]	BLE	Injection-free	-	-	E/T	DoS, MITM
[Antonioli et al., 2020]	BT/BLE	Key.nego downgrade	-	E/T	E/T	Decypt packet, MITM

Table: Security SoA IoT Low Data rates protocols (Sub-GHz, Zigbee, BLE)

Features	CC1356	CC1352R1	STM32WL54CC
Sec. Boot (protection)	✓	✓	✓
Cryptography (protection)	✓	✓	✓
OTA (Update)	✓	✓	✓
Heap ASLR (protection)	✗	✗	✗
Monitoring (detection)	✗	✗	✗
DIFT (hard. monitor)	✗	✗	✗
Code instrumentation (protection)	✗	✗	✗
Anomaly/Intrusion detection	✗	✗	✗

Table: Platform security features comparison

Security Mechanisms

- Confidentiality, Integrity and availability
- Protection mechanisms
- Update & Over the air Mechanisms
- Monitoring & Detection Mechanisms

Figure: CC1352R1 : SoC for IoT

Motivation and contribution

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Contribution: Intrusion Detection System (IDS)

- Acquisition, Analyze and Identification, warn or block attacks

IDS taxonomy

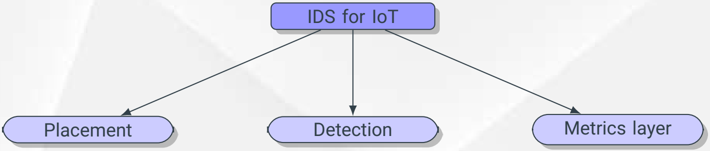
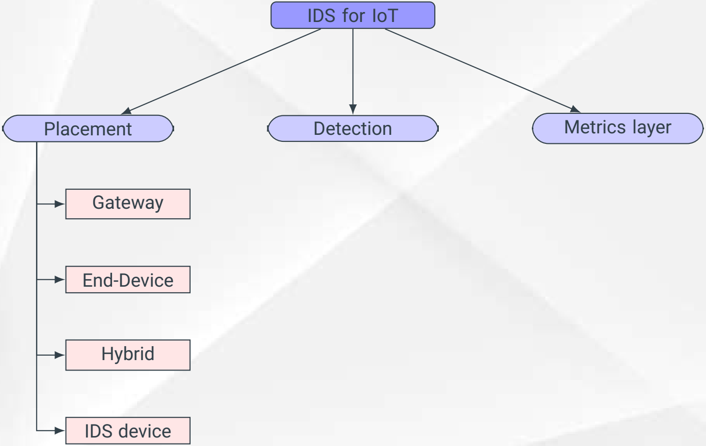


Figure: IDS taxonomy for IoT environment



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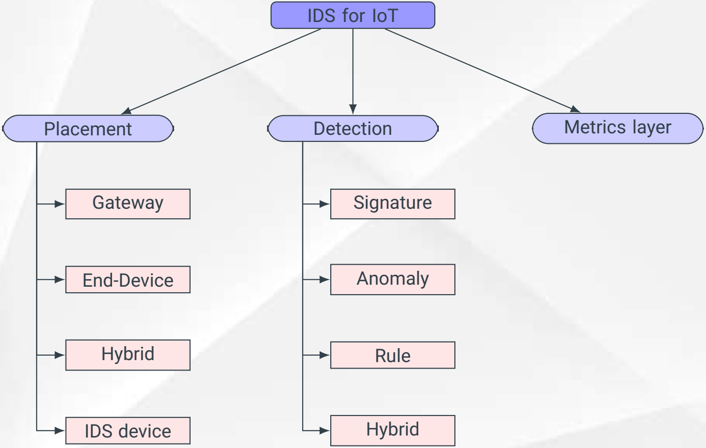

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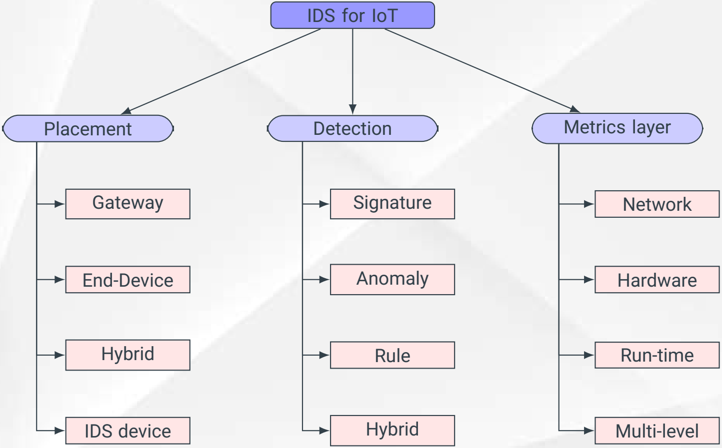

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Host based IDS in state of the art

What are the accurate metrics to be recorded for an HIDS?

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Ref	PHY	MAC	UL	μProc	RT	Target	PS	DM	Place

Table: Host based IDS for IoT

- **MAC** (Mac layer): **TS** (Time series), **P** (Packet Header)
- **UP** (Upper layers): **TS** (Time series)
- **HW** (Hardware/processor) : **IMA** (Illegal memory access), **HPC** (Hardware Performance counter)
- **SW** (Software/runtime): **SC** (Syscalls)
- **Target attacks** : **Spoof** (Spoofing), **Jamm** (Jamming), **P.inject** (Packet Injection), **Rout** (Rooting), **Snik** (Sinkhole)
- **PS** (Proposed Solution): **LKM** (Loadable kernel module), **min.FW** (mini firewall), **ML** (Machine Learning)
- **DM** (Detection Methodology): **B** (Behavior), **S** (signature)
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[Sousa et al., 2017]	-	P	-	-	-	DoS	Analyze & store	S	RC
[Kasinathan et al., 2013]	-	P	-	-	-	DoS, Jamm	SURICATA	S	D
[Eskandari et al., 2020]	Trafic	P	-	-	-	P.inject	GUI LINUX	S	G
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[Gassais et al., 2020]	-	-	-	CTF	-	DD/DoS	Tracing + ML	S	H
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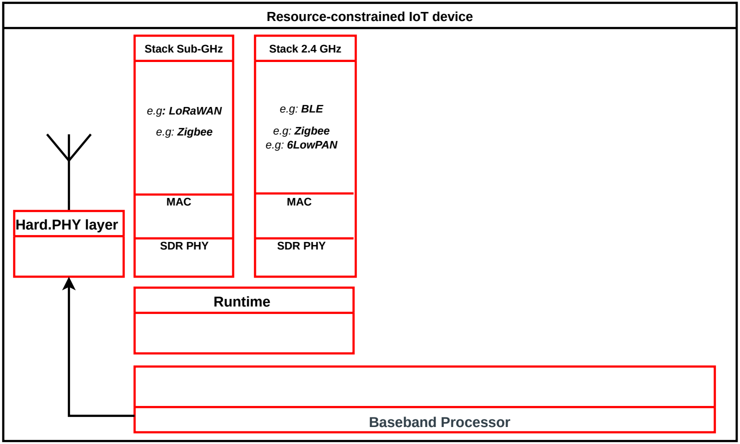
- **MAC** (Mac layer): **TS** (Time series), **P** (Packet Header)
- **UP** (Upper layers): **TS** (Time series)
- **HW** (Hardware/processor) : **IMA** (Illegal memory access), **HPC** (Hardware Performance counter)
- **SW** (Software/runtime): **SC** (Syscalls)
- **Target attacks** : **Spoof** (Spoofing), **Jamm** (Jamming), **P.inject** (Packet Injection), **Rout** (Rooting), **Snik** (Sinkhole)
- **PS** (Proposed Solution): **LKM** (Loadable kernel module), **min.FW** (mini firewall), **ML** (Machine Learning)
- **DM** (Detection Methodology): **B** (Behavior), **S** (signature)
- **Place** (Placement Strategy): **RC** (Resource constraint), **G** :(Gateway), **D** (Device), **H** (Hybrid)

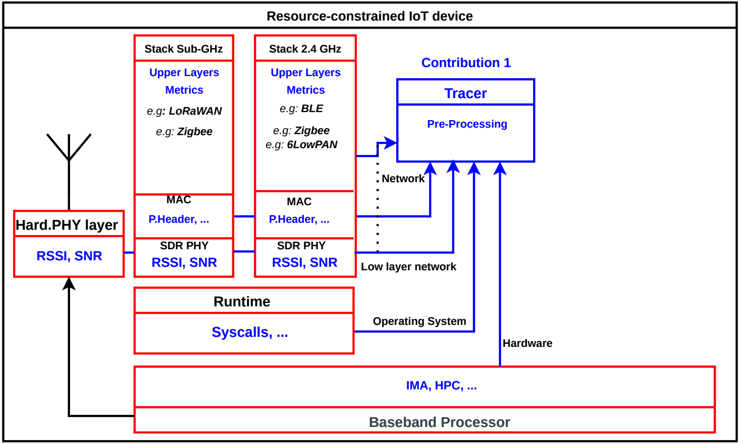
The multi-level approach is not yet addressed in the state of the art

Towards a multi-level metrics HIDS



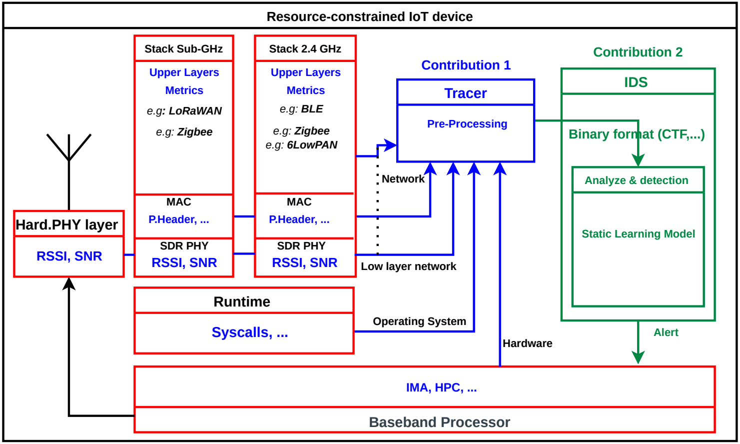
Wireless connectivity block diagram with IDS

Towards a multi-level metrics HIDS



Wireless connectivity block diagram with IDS

Towards a multi-level metrics HIDS



Wireless connectivity block diagram with IDS

Objective

- **Proposed Hardware:**
  - CV32E41P RISC-V Processor for handling the wireless connectivity

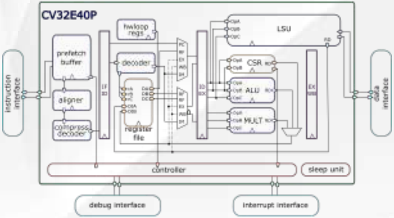


Figure: CV32E41P/40P block diagram

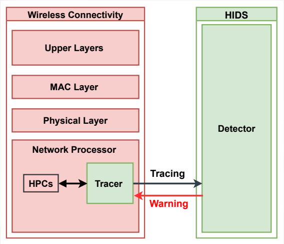
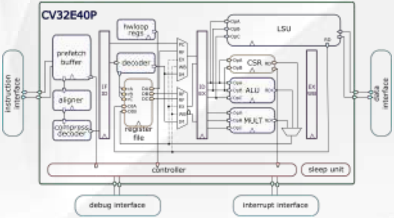


Figure: Testbed block diagram

- **Proposed Hardware:**
  - CV32E41P RISC-V Processor for handling the wireless connectivity
  - Record Hardware Performance Counters (HPC) from CV32E41P by HPMtracer (Hardware block)



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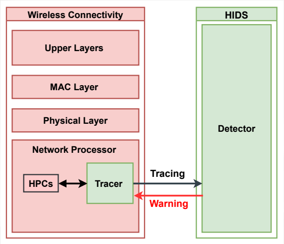

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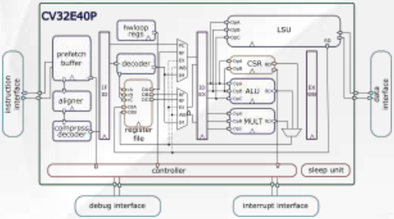
- **Scenario**
  - Reproduction of simple buffer overflow exploit on stack and heap on software running on wireless connectivity part



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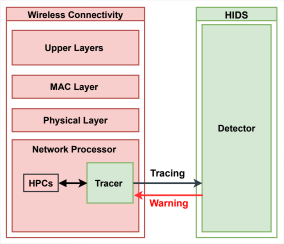

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- **Proposed Hardware:**
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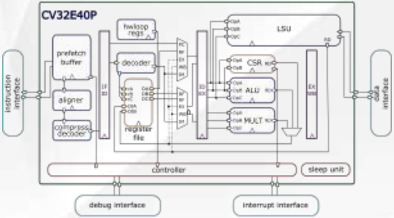
- **Scenario**
  - Reproduction of simple buffer overflow exploit on stack and heap on software running on wireless connectivity part
  - Build Dataset of HPC values per each packet network



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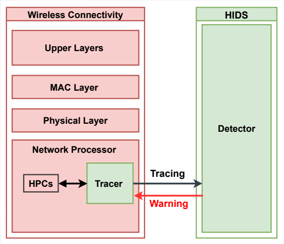


Figure: Testbed block diagram

Test-bed with tracing metrics from RISC-V CV32E41P

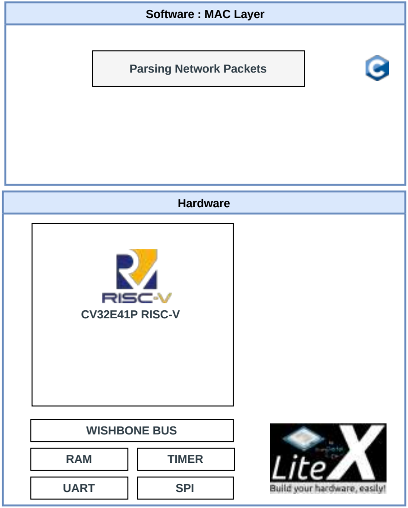
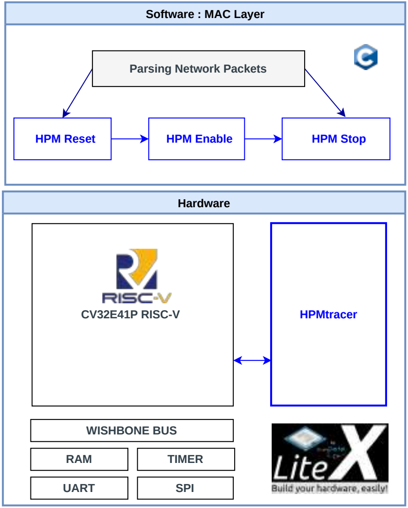


Figure: Test-bed block diagram

Test-bed with tracing metrics from RISC-V CV32E41P



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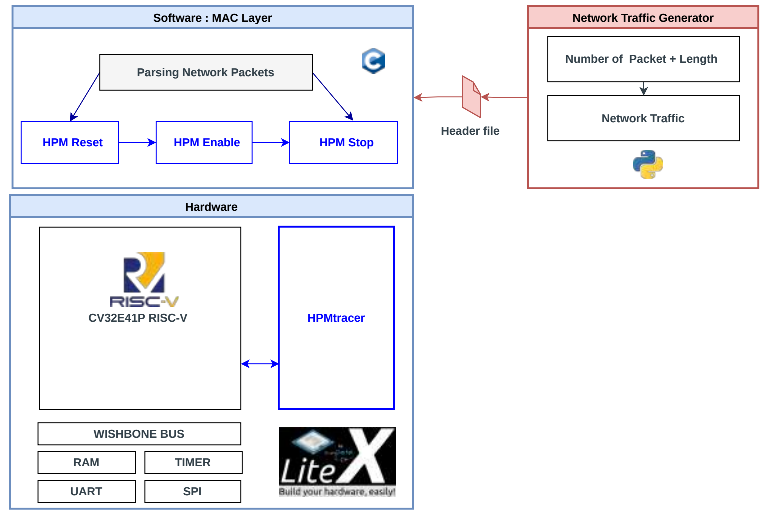

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Test-bed with tracing metrics from RISC-V CV32E41P

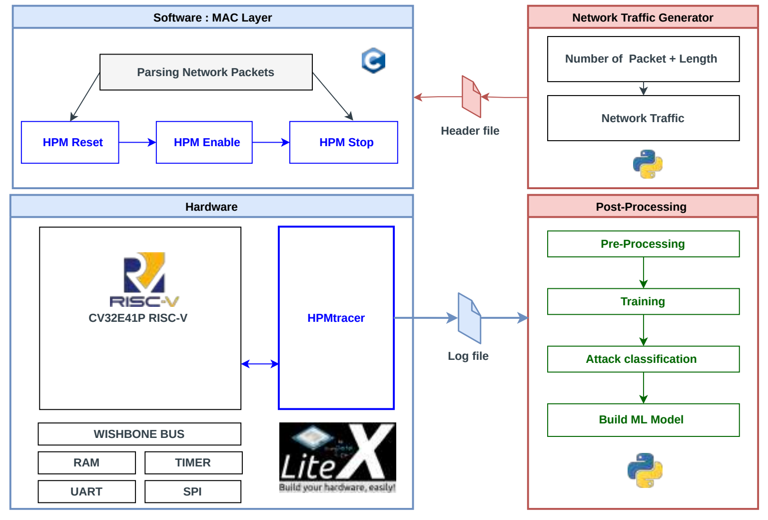

Figure: Test-bed block diagram

Flow diagram

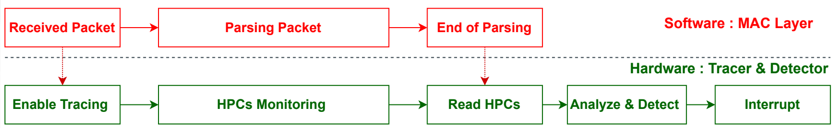

Figure: Flow diagram of network packet processing, HPC monitoring and detection.

Attack Scenarios		Buffer Size	
Packet Type	**Traffic Size**	**Stack**	**Heap**
Legitimate	5 – 10 *bytes*	10 *bytes*	10 *bytes*
S1: Stack Overflow	13 – 23 *bytes*	10 *bytes*	23 *bytes*
S2: Heap Overflow	13 – 23 *bytes*	23 *bytes*	10 *bytes*

Table: The physical buffer size is 10 or 23 bytes. Larger packets result in a buffer overflow.

List of monitored hardware events

Hardware Event	Description	Counter
CYCLES	Number of cycles	0
INSTR	Number of instructions retired	2
LD_STALL	Number of load use hazards	3
JMP_STALL	Number of jump register hazards	4
IMISS	Cycles waiting for instruction fetches	5
LD	Number of load instructions	6
ST	Number of store instructions	7
JUMP	Number of jumps (unconditional)	8
BRANCH	Number of branches (conditional)	9
BRANCH_TAKEN	Number of branches taken (conditional)	10
COMP_INSTR	Number of compressed instructions retired	11

Table: List of hardware events monitored by the CV32E41P performance counters

Shortlisted Hardware Performance Events

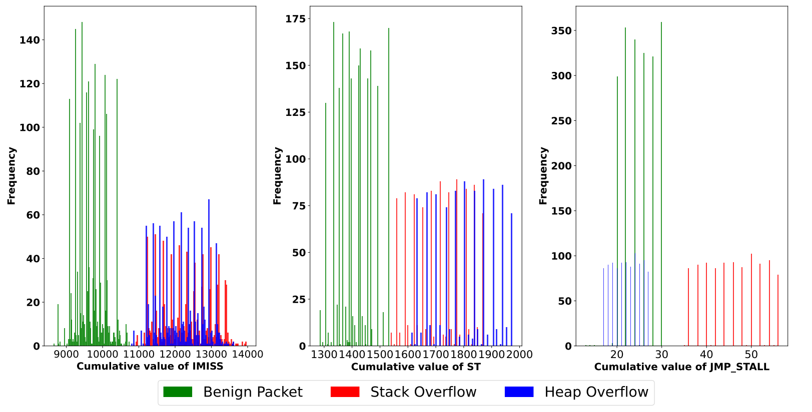

Figure: Distribution of cumulative values of hardware events IMISS, Store and JMP_STALL in attack scenarios

Preliminary results

This histogram shows the evaluation results of the comparison of several classification algorithms.

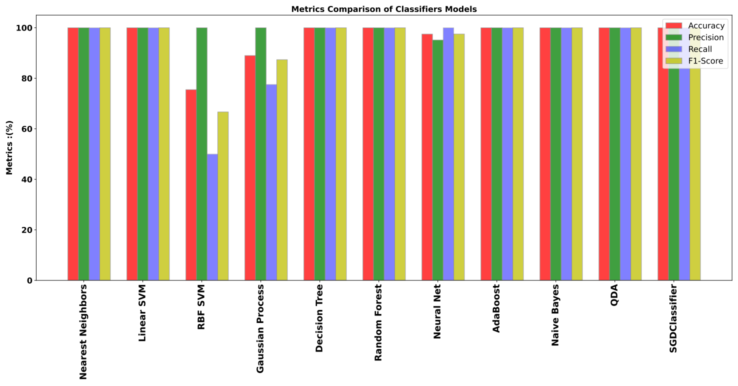

Figure: Comparison of ML Classifiers Models

- Interesting Results
- An in-depth study to follow: Data-set, Scenarios, Detection, Cost?

Generated decision tree classifier model

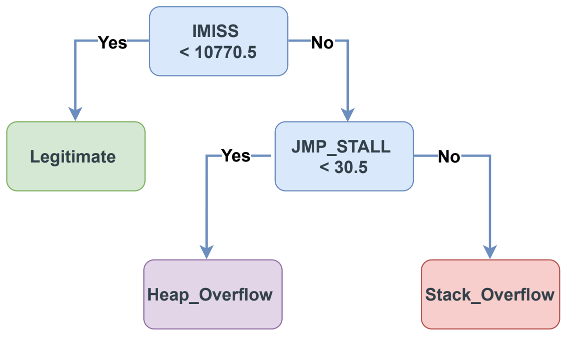

Figure: Generated decision tree classifier model

FPGA Implementation Cost

	HIDS elements			Overhead		Freq	Average Total Power
	HPM (nb)	Tracer	Detector	*LUT*	*FF*	*MHz*	*mW*
V1	✓ (1)	-	-	4636 (+00%)	1237 (+00%)	65.86 (+00%)	91 (+00%)
V2	✓ (2)	-	-	4802 (+3.58%)	1318 (+6.54%)	65.35 (−0.77%)	92 (+1.0%)
V3	✓ (2)	✓	✓	4932 (+6.38%)	1318 (+6.54%)	65.47 (−0.59%)	98 (+7.6%)

Table: Implementation resource utilization and power consumption

Resource Utilization: Arty-A7 35T FPGA

- 6.4%/6.5% of LUTs/FFs Area overhead
- 7.61% Total Power(around 7*mW*)
- 0.6% No impact on the design's performance (65*MHz*)

Prototype with LoRaWAN

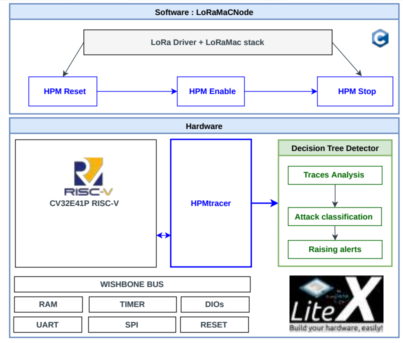

Figure: SoC architecture with LoRaMACnode stack

Figure: Arty-a7 100T FPGA with SX1276 based LoRa shield

Conclusion

- **Ongoing work**
  - New approach for monitoring and detecting remote attacks against IoT devices
  - Simulation Test-bed to detect buffer overflow using hardware counters.
  - Promising results of machine learning classification algorithms.
  - Prototype Testbed with LoRa & LoRaWAN Protocol
- **Future work**
  - Include new features (SNR, RSSI, IAT,. . .) + new attacks (Jamming, . . .)
  - Tracer & IDS Security and Resources Evaluation (Detection, Benchmarks, Overhead, Power consumption).

THANK YOU

Q & A

Requirements and Security Challenges for Resource-Constrained IoT End-Devices Baseband Processor

International Winter School on Microarchitectural Security

Paris, France, December 6, 2022

Mohamed EL-BOUAZZATI, Philippe TANGUY, Guy GOGNIAT

Lab-STICC, Team ARCAD, Université Bretagne Sud

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